Extraction of a Nonlinear AC FET Model Using Small-Signal S-Parameters

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***Abstract*—The nonlinearities of an RF FET can be obtained by a set of small-signal circuit elements extracted over a range of terminal voltages and temperatures. This study used pulsed S-parameter measurements on a 3×3 dc-bias-point grid at two different temperatures to obtain electrical and electrothermal nonlinearity coefficients up to the third order. The extracted nonlinear ac model can be used in Volterra analysis to gain an insight into distortion mechanisms. The measurement results were in good agreement with the calculated third-order intermodulation values.**

***Index Terms*—Nonlinear characterization, nonlinearity, pulsed S-parameter measurements, S-parameters, self-heating, third-order intermodulation, Volterra model.**

I. Introduction

MUCH EFFORT has been put into developing accurate small-signal simulation models for RF FETs, and accurate small-signal extraction procedures have been developed up to 10 GHz [1]. The standard extraction procedure is based on measured S-parameters that are first converted to Y-parameters. After deembedding extrinsic components, the circuit elements of the transistor can then be calculated using analytical equations.

Linearity is one of the key requirements in modern telecommunication systems. To improve the linearity, it is necessary to simulate nonlinear effects in FETs, and nonlinear device characterization is needed. This paper extends well-known small-signal characterization methods into nonlinear characterization. The procedure is based on a set of small-signal circuit elements extracted over a range of bias voltages and temperatures, and the nonlinearities of the circuit elements are calculated from neighboring measurement points. This method enables third-order polynomial characterization and allows the simulation of third-order intermodulation (IM3) distortion generated by electrical and electrothermal distortion mechanisms. The method can also be used to simulate the effects of envelope and harmonic impedances in FET amplifiers.

Section II shows the procedure for extracting polynomial nonlinearities from small-signal circuit parameters, while Section III describes pulsed S-parameter measurements designed to avoid self-heating and discusses the effects of pulselength. In Section IV, nonlinear characterization is applied to an Infineon CLY2 MESFET. Section IV further presents linearity calculations for a common-source amplifier using an analytical Volterra model. The results show good agreement between modeled and measured data.

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II. Nonlinear Characterization

The nonlinear characterization of RF transistors and amplifiers has attracted a lot of attention in recent years. Research in the area has two major approaches: empirical and physical. Empirical models, such as the nonlinear model with memory presented in [2], do not contain information about internal device operation. The output of the amplifier is considered as a memoryless two-dimensional function of input and output voltages, and memory is produced by input and output filters. The filters and two-dimensional transconductance are extracted from small-signal s-parameter measurements performed over a range of frequency and bias voltage values [2]. The addition of filters is an important step toward modeling a nonlinear amplifier with memory, but it must be noted that the filters fail to characterize memory correctly. For example, internal frequency-dependent feedback produced by the transistor connects nonlinear responses back to the input. Effects such as these tend to be neglected in those kinds of models.

In physical models, every parameter has some form of physical significance. These models provide information about internal device operation and are good at predicting fundamental signal properties [3], [4] over a wide range of frequency. However, nth-order derivatives of the curves must be accurate for nth-order distortion simulations. Since physical models are constructed such that one fixed equation covers all operation regimes, derivatives of the curves are usually not accurate over the whole range of bias values, causing errors in distortion simulations.

This paper proposes a nonlinear model of a common-source FET amplifier. The model, presented in Fig. 1, is a conventional small-signal model, but the most nonlinear circuit elements are considered polynomial. In contrast to the empirical model presented in [2], the proposed model is based on a small-signal model, which is proven to be accurate over its frequency range. Compared to the physical models presented in [3] and [4], this model is fitted locally to make all derivatives as accurate as possible with the chosen bias values. The model takes account of nonlinearities produced by transconductance, output conductance, cross terms, Cgs and Cgd, including their dynamic temperature dependencies. In addition, the extraction procedure is capable of dealing with more complicated models and a larger

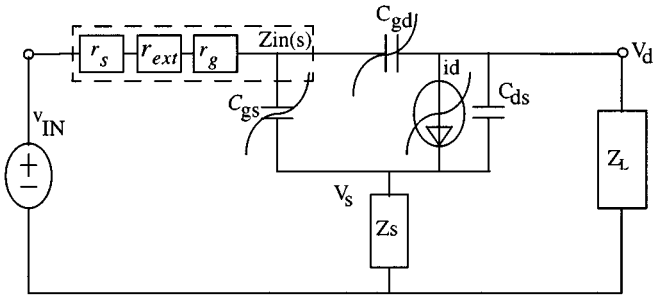


Fig. 1. Model of the common-source FET amplifier.

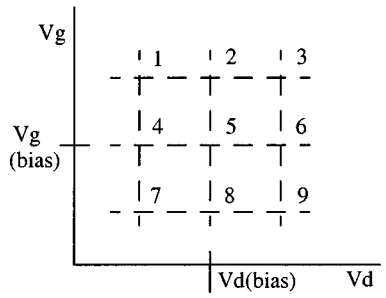


Fig. 2. Principle of nonlinear S-parameter characterization.

number of nonlinearities. A polynomially modeled drain current up to the third order can be expressed by

$$\begin{aligned} i_D = {} & gm\cdot\nu_g + K2gm\cdot\nu_g^2 + K3gm\cdot\nu_g^3 + go\cdot\nu_d \\ & + K2go\cdot\nu_d^2 + K3go\cdot\nu_d^3 + K2gmgo\cdot\nu_g\cdot\nu_d \\ & + K3gm2go\cdot\nu_g^2\cdot\nu_d + K3gmgo2\cdot\nu_g\cdot\nu_d^2 \\ & + K3Tgm\cdot T\cdot\nu_g + K3Tgo\cdot T\cdot\nu_d + K2T\cdot T. \end{aligned} \quad (1)$$

The drain current of an FET is considered as a three-dimensional function of gate and drain voltage and temperature. Temperature, in turn, is regarded as an independent low-frequency variable because chip temperature may vary at the envelope frequency, causing changes in circuit element values and intermodulation (IM) distortion. The dissipated power spectrum includes a number of frequencies, but only their dc and envelope components fit into the thermal impedance passband. This agrees well with low-frequency approximations for chip temperature variations. Since the dc and envelope components are second-order signal components, the addition of just three more terms into (1) enables it to model temperature effects up to the third order.

As the extraction procedures for different nonlinearities are basically identical, this paper extracts the coefficients presented in (1) as an example. First, partial derivatives of vg and vd without temperature effects can be expressed by

$$\begin{aligned} \frac{\partial i_D}{\partial \nu_g} = {} & gm + 2\cdot K2gm\cdot\nu_g + 3\cdot K3gm\cdot\nu_g^2 + K2gmgo\cdot\nu_d \\ & + 2\cdot K3gm2go\cdot\nu_g\cdot\nu_d + K3gmgo2\cdot\nu_d^2 \end{aligned} \quad (2)$$

and

$$\begin{aligned} \frac{\partial i_D}{\partial \nu_d} = {} & go + 2\cdot K2go\cdot\nu_d + 3\cdot K3go\cdot\nu_d^2 + K2gmgo\cdot\nu_g \\ & + 2\cdot K3gmgo2\cdot\nu_g\cdot\nu_d + K3gm2go\cdot\nu_g^2. \end{aligned} \quad (3)$$

Equations (2) and (3) correspond to the extracted small-signal gm and go. Fig. 2 shows the rectangular 3×3 grid of measurement points used here, and the measured data matrix can be written by

$$Y = [gm1 \quad go1 \quad gm2 \quad go2 \quad \cdots \quad gm9 \quad go9]^T \quad (4)$$

and, by applying (2) and (3) at all nine data points, the following 18×9 matrix can be set up as (5), shown at the bottom of this page. As a result, we have 18 equations and nine unknown nonlinearity coefficients. These extra equations provide a large degree of useful redundancy for characterization. Solving the matrix by means of least mean square error (LMSE) fitting enables the extraction of nonlinearity coefficients (6). A rectangular grid presented in Fig. 2 is used here for simplicity, but other kind of grids can also be used.

$$\mathrm{COEFFS} = \left((C^T\cdot C)^{-1}\cdot C^T\right)\cdot Y. \quad (6)$$

III. Effects of Chip Temperature

The extraction of nonlinearities is impeded by variations in chip temperature. Steady-state measurements show that the temperatures in all points in Fig. 2 are different. Thus, it is extremely difficult to extract nonlinearities on the basis of these measurement points since it is impossible to establish which part of the nonlinearity is caused by voltage and which part is caused by temperature variations. To avoid the effects of self-heating, S-parameter measurements must be carried out using such short pulses that the chip has no time to heat up [5].

Fig. 3 presents the test setup for the pulsed S-parameter measurements. At time zero, the gate-bias voltage is triggered from the pinchoff to the correct value and, depending on the values of the bias inductors, an electrical steady state will be shortly obtained. The network analyzer (NWA) measures one S-parameter

$$c = \begin{bmatrix} 1 & 2V_{G1} & 3V_{G1}^2 & 0 & 0 & 0 & V_{D1} & 2V_{G1}V_{D1} & V_{D1}^2 \\ 0 & 0 & 0 & 1 & 2V_{D1} & 3V_{D1}^2 & V_{G1} & V_{G1}^2 & 2V_{G1}V_{D1} \\ \vdots & \vdots & \vdots & & & & & & \\ 1 & 2V_{G9} & 3V_{G9}^2 & 0 & 0 & 0 & V_{D9} & 2V_{G9}V_{D9} & V_{D9}^2 \\ 0 & 0 & 0 & 1 & 2V_{D9} & 3V_{D9}^2 & V_{G9} & V_{G9} & 2V_{G9}V_{D9} \end{bmatrix} \quad (5)$$

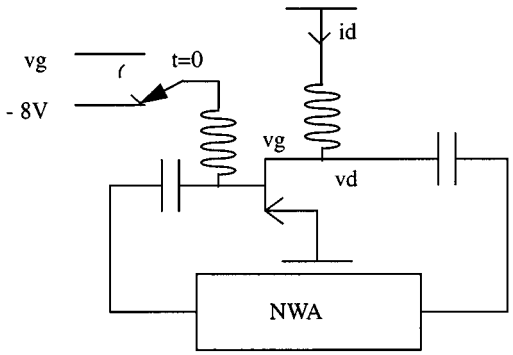


Fig. 3. Test setup for pulsed S-parameter measurements.

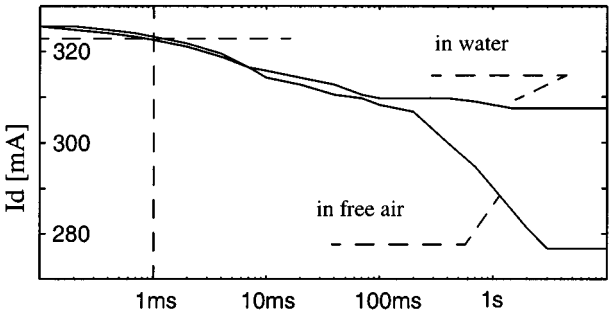


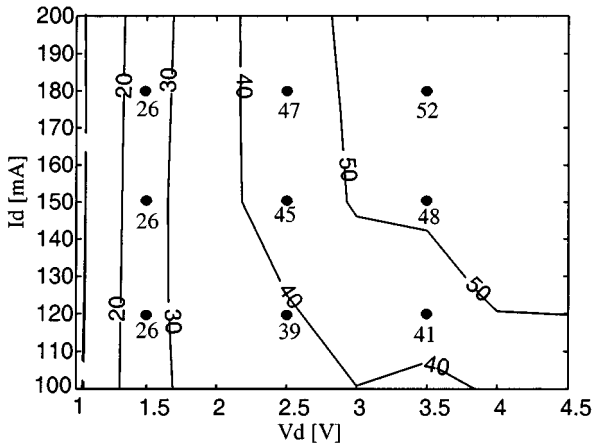
Fig. 4. Thermal step response of the CLY2 chip and package.

at the time and, by repeating the measurement four times, all the S-parameters will be obtained at one bias point. The nonlinear characterization of S-parameters is completed by sweeping the terminal voltages and temperatures at constant frequency.

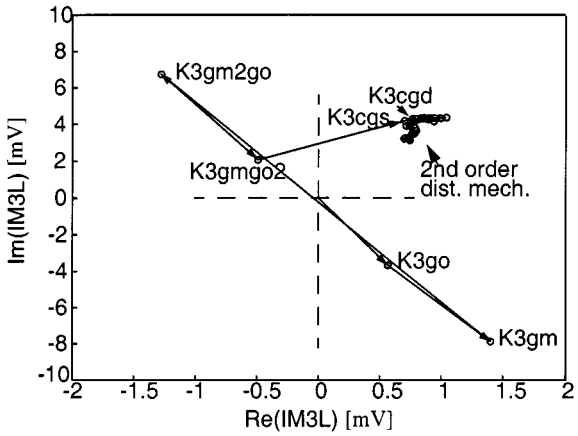
Among the most important considerations in pulsed measurements are the effects of pulselength. The pulse must be sufficiently long to produce an electrical steady state, while at the same time, it must be as short as possible to minimize self-heating. The thermal time constants of the Infineon CLY2 chip and package used in this experiment were measured by triggering the gate voltage to zero, and then monitoring the drain current as a function of time. As changes in drain current indicate changes in chip temperature, thermal settling times up to 3 s can be obtained without a heat sink. If the chip is immersed in water, the largest settling time is 100 ms, as seen in Fig. 4. In both cases, 1 ms is a sufficiently short measurement time because changes in the drain current of a packaged CLY2 transistor occur mostly after 1 ms. However, it is evident that self-heating cannot be completely avoided even by 1-ms pulses, particularly at high dissipated power values. As a result, some errors will inevitably occur due to the small time constants of the semiconductor material. On the other hand, it is important to emphasize that the time constants of the package are large and its total thermal impedance is high. Hence, 1 ms is much closer to the isothermal than the steady-state situation, as indicated by the measurements shown in Fig. 4.

The extraction starts from the actual bias voltage values, which provide a basis for calculating the correct chip temperature as follows:

$$T = T_{\mathrm{AMB}} + R_{\mathrm{TH}} \cdot V_D \cdot I_D \cdot (1 - \eta) \tag{7}$$



(a)



(b)

Fig. 5. (a) Linearity contours and measured points for the lower IM3 sideband in decibels related to carrier (dBc). (b) Vector representation of IM3L components at 2-MHz tone spacing.

where T_{AMB}, R_{TH}, and η are the ambient temperature, thermal resistance, and efficiency of the amplifier. Next, the values of the small-signal circuit elements, including elements at neighboring voltages, are calculated to correspond to that chip temperature, by interpolating the extracted element values at two temperature values. As the electrical extraction procedure presented in Section II is now applied to these interpolated constant temperature elements, the electrothermal nonlinearity coefficient $K3goT$, for example, can be calculated by the following:

$$k3goT = \frac{\overline{go(T2)} - \overline{go(T1)}}{(T2 - T1)} \tag{8}$$

where $T1$ and $T2$ are temperature values, and go values represent mean values over the drain voltage extraction range. $K2T$ describes temperature-dependent changes in drain current and $K3gmT$ models the combined effects of temperature and gate voltage. Similar equations can be devised for these electrothermal nonlinearity coefficients.

IV. Linearity Simulations

An Infineon CLY2 GaAs MESFET was characterized by the S-parameter characterization method. The extracted polynomial nonlinearities were used in distortion simulations

TABLE I
NONLINEARITY COEFFICIENTS AND CIRCUIT COMPONENTS OF CLY2

gm=0.14	K2gm/gm=0.048	K3/gm=-0.025
go 0.0174	K2go/go=-0.056	K3go/go=-0.014
K2gmgo/go=-0.12	K3gm2go/go=-0.29	K3gmgo2/go=-0.040
K2T=0.00041	K3gmT=0.000044	K3goT=0.000020
cgs=2.2pf	K2cgs/cgs=0.095	K3cgs/cgs=0.010
K2Tcgs=-0.0015	K3Tcgs=-0.011	
cgd=0.22pf	K2cgd/cgd=-0.0073	K3cgd/cgd=0.0001
K2Tcgd=-0.0022	K3Tcgd=-0.0004	
cds=0.53pf		

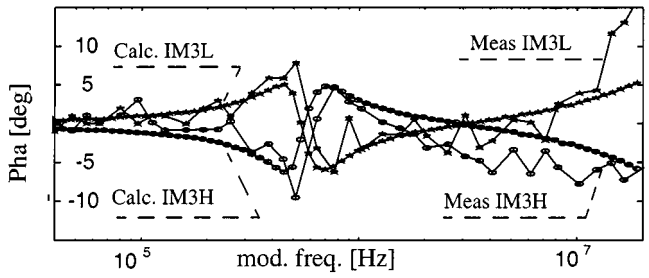


Fig. 6. Calculated and measured phase of IM3 components as a function of tone difference.

of real amplifier using Volterra series. As [6] and [7] provide a detailed description of the model, suffice to say here that it regards nonlinearities as current sources connected in parallel with linearized small-signal elements, and that the current of the source depends on the nonlinearity coefficient and voltages used. The method allows the analytical calculation of distortion components in accordance with linear circuit theory.

The Volterra calculated IM3 products over the range of bias voltages at the center frequency of 1.8 GHz and modulation frequency of 2 MHz, while the output voltage swing was 2 Vpp. The results, shown in Fig. 5(a), indicate a reasonably good correlation between the two.

One of the major advantages of the Volterra model is that distortion products can be presented as the sum of individual distortion mechanisms. To provide an example, we shall study linearity at the drain and gate voltage values of 4.5 V and 150 mA in more detail. Table I presents the values of the circuit elements and the nonlinearity coefficients, and Fig. 5(b) represents the simulated lower third-order intermodulation (IM3L) vector in real-imaginary coordinates. Starting at the origin and ending at $+0.5 - j3$ mV, $K3go$ is the first nonlinearity mechanism. $K3gm$ has approximately the same amplitude and phase as $K3go$. Since gm and go are highly linear at high drain bias voltage and current values, $K3gm2go$ is the dominating nonlinearity mechanism. As $K3gmgo2$ also plays a prominent role, these four nonlinearities can be considered as the predominant causes of distortion, even though the effects of the input nonlinearity $K3cgs$ cannot be ignored. In addition, the second-order distortion mechanisms converting from the envelope ($w2-w1$) and second harmonic ($2w1$) frequencies also have a significant impact, causing approximately 15% of IM3L distortion.

At the next stage, the tone-difference of a two-tone signal was swept, and the phase of the calculated and the measured [8] IM3 components were compared. It should be emphasized that this comparison is a very strict figure-of-merit for the validity of the model and the extraction procedure because small deviations in the phase of IM3 are caused by interaction among a number of distortion mechanisms. Fig. 6 shows the phase of the IM3L and higher third-order intermodulation (IM3H). As can be seen, the calculated and measured data are in very good agreement. The resonance in phase response at 500 kHz is caused by resonance in load impedance at that frequency caused by the *LC* time constant in the bias network, while the phase drift at very high modulation frequencies is caused by nonconstant gate impedance at the envelope frequency.

V. SUMMARY

This paper has extended the small-signal S-parameter characterization of RF FETs to include the effects of nonlinearities. The extraction procedure discussed is based on small-signal circuit components extracted over a range of terminal voltages and temperatures. This paper has also presented matrix equations for solving polynomial nonlinearity coefficients.

The problem of self-heating is avoided by using pulsed S-parameter measurements with a pulselength of 1 ms. This pulselength is sufficiently long to achieve an electrical steady state, while being short enough to avoid over 85% of self-heating in a packaged CLY2 transistor. The CLY2 is simulated in a common source configuration with an analytical Volterra model, and the results show good agreement between modeled and measured data.

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